High-speed SRAM Cache Design Review 2

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ABSTRACT

This paper serves as an effective intermediate design review to convince the PICo board that our team has made substantial progress in the design of our high speed 64KB SRAM cache. Specifically, this report will include an updated schedule detailing the completion timeline of the project, a block diagram detailing high level status of our design, a block diagram of the model we used for our simulations, a diagram of our bitcell layout, and HOLD and READ butterfly graphs with the correct Static Noise Margin (SNM) calculations at each process corner.

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1. SCHEDULE

Our original schedule is shown below (Table 1) and depicts the design timeline we initially created.

Table 1. Proposed timeline for Project

Dates	Completion
Oct 23	Complete SKILL Tutorial
Oct 30	Functioning SRAM; Optimization methods
Nov 13	Optimizations decided and implemented
Nov 18	Paper draft & compile
Nov 27	Final design & paper
Dec 2	Presentation practice

This schedule was sufficient as a high level timeline with which to organize our thoughts at the beginning of the project. However, as the project evolves we have found it useful to revise the schedule to not only make it more detailed, but to also accommodate design challenges and revisions which were unforeseen. Below is the updated, detailed schedule for the rest of the project (Table 2).

Table 2. Revised timeline for Project

Dates	Completion
Nov 16	Submit Design Review 2
Nov 19, 20	Research optimization techniques for our SRAM cell, Document and share findings
Nov 26	Begin work on Final Design Review Includes: Testing, simulation, optimizations, updates for logical effort, decoupling address decoders
Nov 27	Implement testing on the maximum data transfer modes of the architecture to meet PICo's design requirements for high speed cache
Nov 28-30	Finalize simulations and functionality, ensure design can operate at specified metrics (Energy, delay, power,
Dec 3-7	Complete Design, begin writing final document and preparing for the presentation. Includes creating slides, finalizing calculations and ensuring all circuit functionality
Dec 10	Final Presentation and defense of design

We have met our schedule up to the second design review. Some design decisions had to be postponed in the interest of time. For example, our logical effort calculations are pending until we make a final decision about how we are going to orient our SRAM block. We are still in the process of determining the optimum bitcells per row and column. This will affect the logical effort. Consequently, we will address logical effort for the final design review. As mentioned above, we are still in the process of determining which orientation of rows and columns is most effective. To do this, we plan to run simulations that analyze the total delay (t_{plh} and t_{phl}) for various orientations of the rows and columns. From there, we will be able to determine the optimum orientation of our SRAM.

As we look toward the final design review, our focus will be on optimizing the functional SRAM we currently have. This will include determining the most effective sizing for each component (SRAM bitcells and peripheral circuits). By achieving ideal sizing, we will improve the power consumption, energy efficiency and overall speed of our circuit. To do this, our team will heavily focus on simulation and hand calculations to ensure our optimizations are in fact the best we can achieve. We will also begin to consider how fast we want to clock our SRAM. To do this, we will look at current technologies and scale our clock speed appropriately. We will also begin developing a full size layout for our SRAM. This layout will be as tight as possible

where the components are concerned and will implement all of our optimizations.

2. PROGRESS & REMAINING CHALLENGES

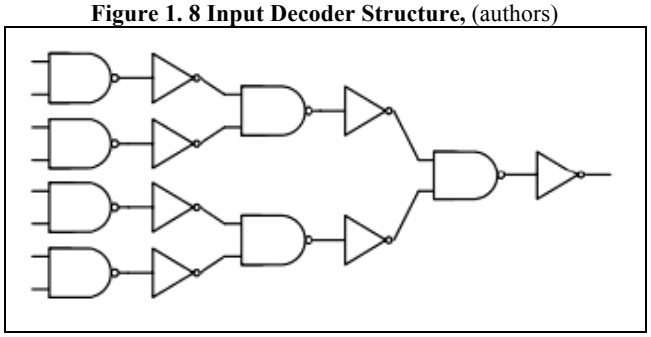
We made significant progress toward our final design for this Review. Specifically, we have finalized block diagrams, a functioning SRAM circuit with simulations, and the SNM calculations for 5 process corners (TT, FF, FS, SF, SS) during the Hold and Read operations of the circuit.

2.1 Block Diagrams and Peripheral Circuits

Our physical block diagrams are appended and titled at the end of this document (Fig. 2, Fig.3). As we begin our work for the final design review, we may think about altering our architecture. Specifically we are interested in knowing if breaking up the address and row decoders, and chunking up the circuit will increase the speed of our SRAM. After meeting with Professor Stan and discussing the benefits and costs associated with this design change, we will approach this area with careful documentation and fore-thought.

Currently, we have an 8-bit decoder implemented through a 4-to-16 pre-decoding stage and a decoding stage. Transistor sizing are found using logic effort. This implementation is faster than the 256 AND gates structure. To further improve the performance of the decoders, we will use 6-stage breakdowns of the 8-input AND (Fig. 1):

Figure 1. 8 Input Decoder Structure, (authors)



Total fanout on each address wire is:

$$F = B*Cout/Cin = 128*(256Ccell)/(4*Ccell) = 2^{13}$$

Using the above 2-input NAND gates:

$$\text{Total LE} = (4/3)^3 = 2.4$$

$$PE = 2.4 * 2^{13}$$

Sizing of gates will also be determined using logic effort. Optimal N is around 7.1

2.2 SRAM Functionality

We were able to calculate the read access time and the write access time for our SRAM. Those values are as follows:

Read Access Time = 69.42 picoseconds
Write Access Time = 976 picoseconds

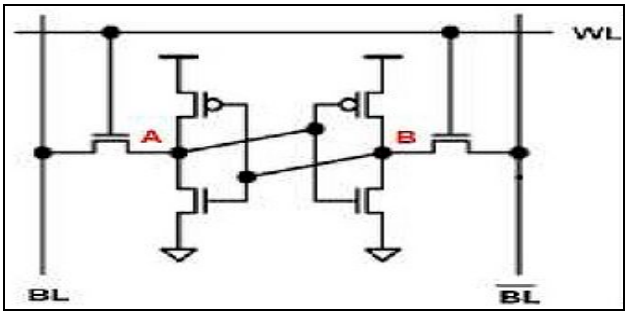
The read access time is significantly shorter than the write time. This discrepancy is attributed to the battle during the write between a weak transmission gate internal to the circuit, a large access transistor, and a pull down transistor inside the cell. In order to decrease the difference between our read and write access times, we will increase the size of the transistors in question to drive the proper times. By increasing the size of these drivers we will be able to decrease our write access time.

Another challenge we will confront heading into the final design stages is that of our pre-charge driver and peripheral circuits. Our pre-charge driver is relatively weak compared to the cells. When analyzing data on the 4-bitcell simulation we noticed that turning on the word line significantly dips the other bit lines. To mitigate this issue, we will modify the transistor sizes in our bitcell to make this voltage loss smaller. In doing so, we will improve our reads and writes, and save power. By addressing these design issues we will ensure that our circuit is optimized for speed heading into the final design.

2.3 SNM Analysis

A major milestone of this design review was the successful simulation of the SNM for each process corner during a hold and read operation. To do so, we configured our simple bitcell in the Cadence simulation environment (Fig. 1)

Figure 2. Simple SRAM 6T Bit Cell *(U.Va ECE wiki)*



In order to successfully simulate the butterfly curve, we drove node A from 0 to VDD, and observed and plotted the effects on node B. Similarly to simulate the second part of the butterfly curve, node B was driven from 0 to VDD and node A was observed and plotted. In graphical form, the independent variable was plotted on the x-axis, while the observed variable was plotted on the y-axis. Exporting this data from Cadence, we were able to manipulate it in Excel to rotate the graph 45 degrees using trigonometric transformations. From this graph, we were able to calculate the difference between the two curves at any given x value. We compared the absolute value of the maximum and minimum differences, and selected the smaller of the two as our SNM. This simulation was conducted both for the Read case (WL=1), and the Hold case (WL=0). Furthermore, we performed this simulation at all 5 process corners (temperature and vdd) for both Read and Hold. (TT = 27C, 1.1V; FF = 0C, 1.2V; SS = 50C, 1.0V; FS = 0C,1.0V; SF = 50C,1.2V). This process was detailed in the tutorial on the U.Va ECE Wiki page [1]. The values we obtained are organized in Table 3 and Table 4.

Table 3. SNM Measurements, Hold Operation

Process Corner	SNM
TT	.31589
FF	.34079
SS	.29648
FS	.31712
SF	.31356

Table 4. SNM Measurements, Read Operation

Process Corner	SNM
TT	.26900
FF	.28419
SS	.25766
FS	.27323
SF	.26285

3. TASK BREAKDOWN

The contributions of each team member are described in detail below:

Drew – for this design review, I focused on the simulation of a bit cell to verify functionality and gather necessary metrics. I built a test bench with a bit cell and the relevant peripherals to verify things were functional and created an ocean script to allow for quick aggregation of these metrics whenever we change the sizing or architecture of our circuit. I also did a simple simulation to calculate the effective capacitance looking into the word lines and bit lines of a cell, so that when simulating we can approximate the effect of 255 other bit cells on the same bit/word lines as the bit line in simulation.

Chuhong – For this design review, I developed the overall SRAM structure, the block diagram showing our project progress and the mock simulation block diagram. Currently we have our SRAM block 256*256 (row*column) bitcells. According to initial simulations, square structure gives us the best delay. Next step, we need to take into account the peripherals (row/column decoder and deMUX implementations) to find the optimal row/column structure. I also conducted research on 8-bit address decoders and wrote the netlist.

Lauren – I worked extensively on the simulation and analysis of the SNM graphs. To do this, I performed simulations on one of our pre-designed bit cells in the Cadence simulation environment. For the simulations I spent time setting up and configuring each process corner as well as figuring out how to drive a variable voltage through our circuit. Once I had the ADE L testing environment successfully setup, I was able to get the butterfly curves at each process corner. The next challenge was figuring out how to calculate the appropriate SNM values from the butterfly curves. I worked with Rebecca to extract the butterfly curve values into an excel spreadsheet where we could easily perform large calculations on the data. Doing this allowed us to quickly find the maximum and minimum rectangle values between the curves and calculate the SNM value. I was primarily in charge of finding the SNMs at each process corner for the Read Operation.

Rebecca – I worked extensively with Lauren to simulate, plot and calculate the SNM values for our circuit. I followed the same procedure that Lauren described above. I worked to find the SNM values for the Hold Operation. I also compiled and organized the Design Review Report. This consisted of collecting and understanding all the simulations, calculations and block diagrams and documenting our procedures so they were understandable.

4. REFERENCES

[1] U.Va ECE Wiki, *http://venividiwiki.ee.virginia.edu/*

4. SIMULATION FIGURES

Figure 3. Simulation Block Diagram

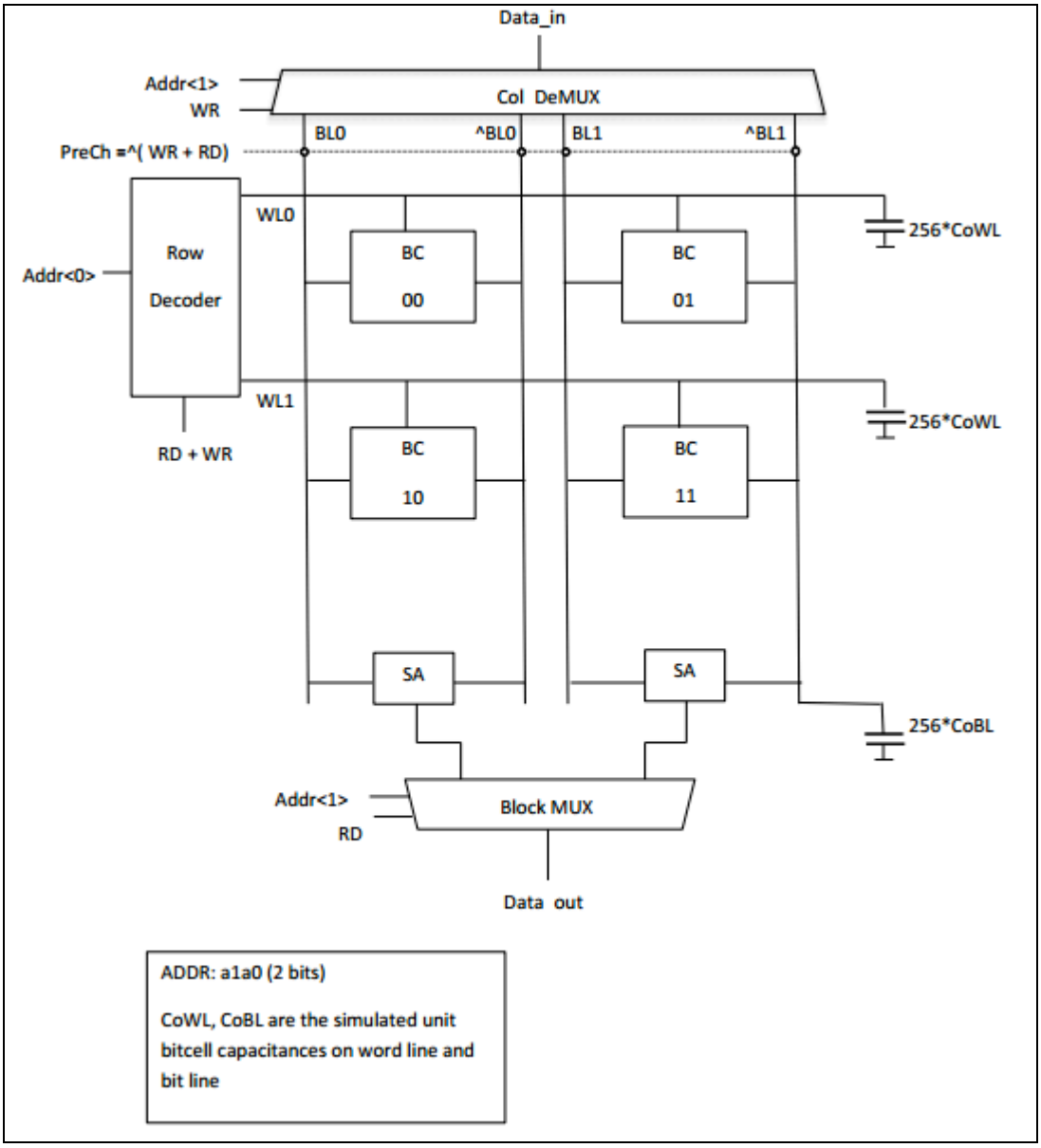


Figure 3. Block Diagram Color Coded with Status Indicators

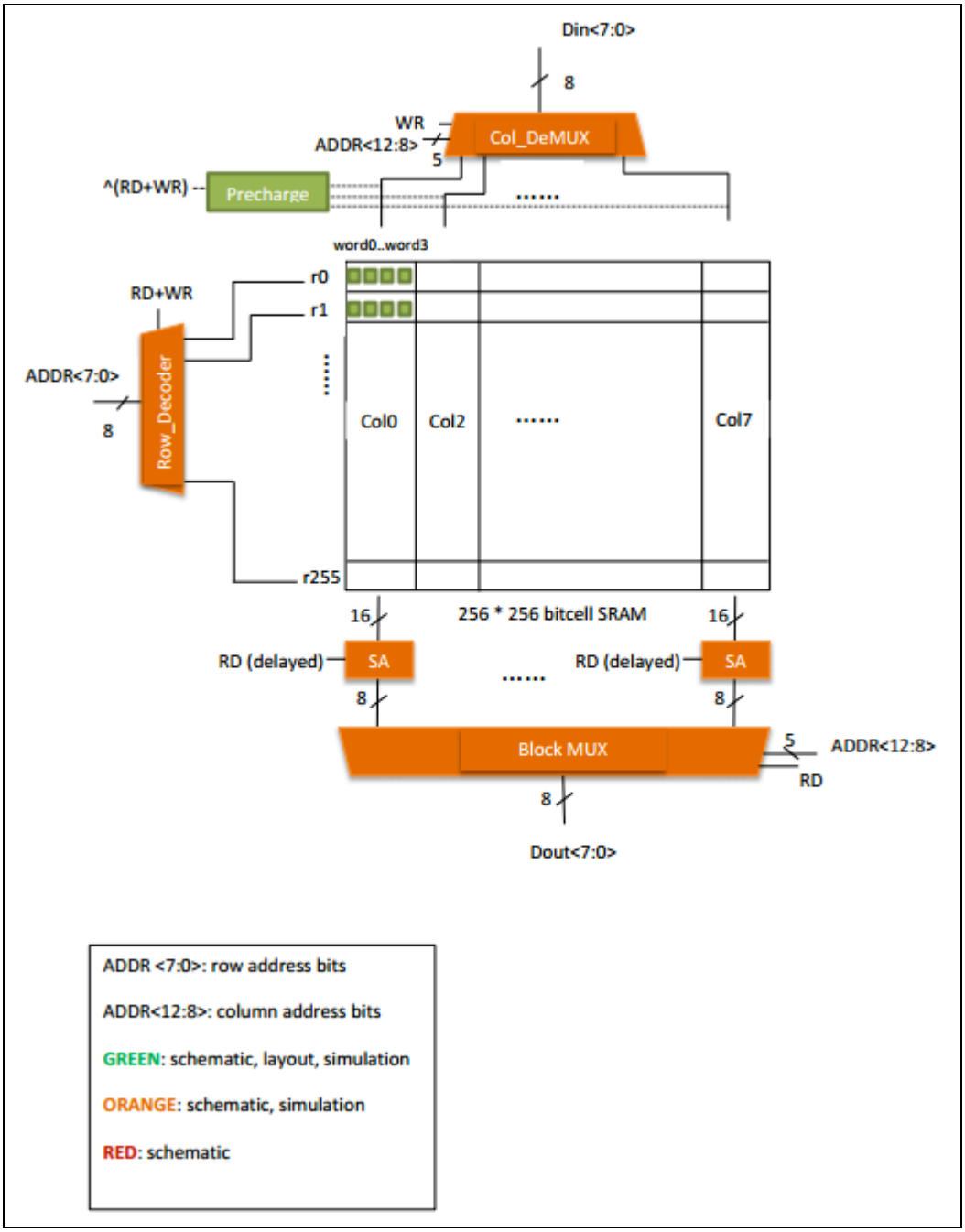

Din<7:0>
8
WR
ADDR<12:8>
5
Col_DeMUX
^(RD+WR) --
Precharge
word0..word3
RD+WR
r0
r1
ADDR<7:0>
8
Row_Decoder
Col0
Col2
Col7
r255
16
256 * 256 bitcell SRAM
16
RD (delayed)
SA
RD (delayed)
SA
8
8
Block MUX
5
ADDR<12:8>
RD
8
Dout<7:0>
ADDR <7:0>: row address bits
ADDR<12:8>: column address bits
GREEN: schematic, layout, simulation
ORANGE: schematic, simulation
RED: schematic

Figure 3. Successful SRAM Functionality Simulation

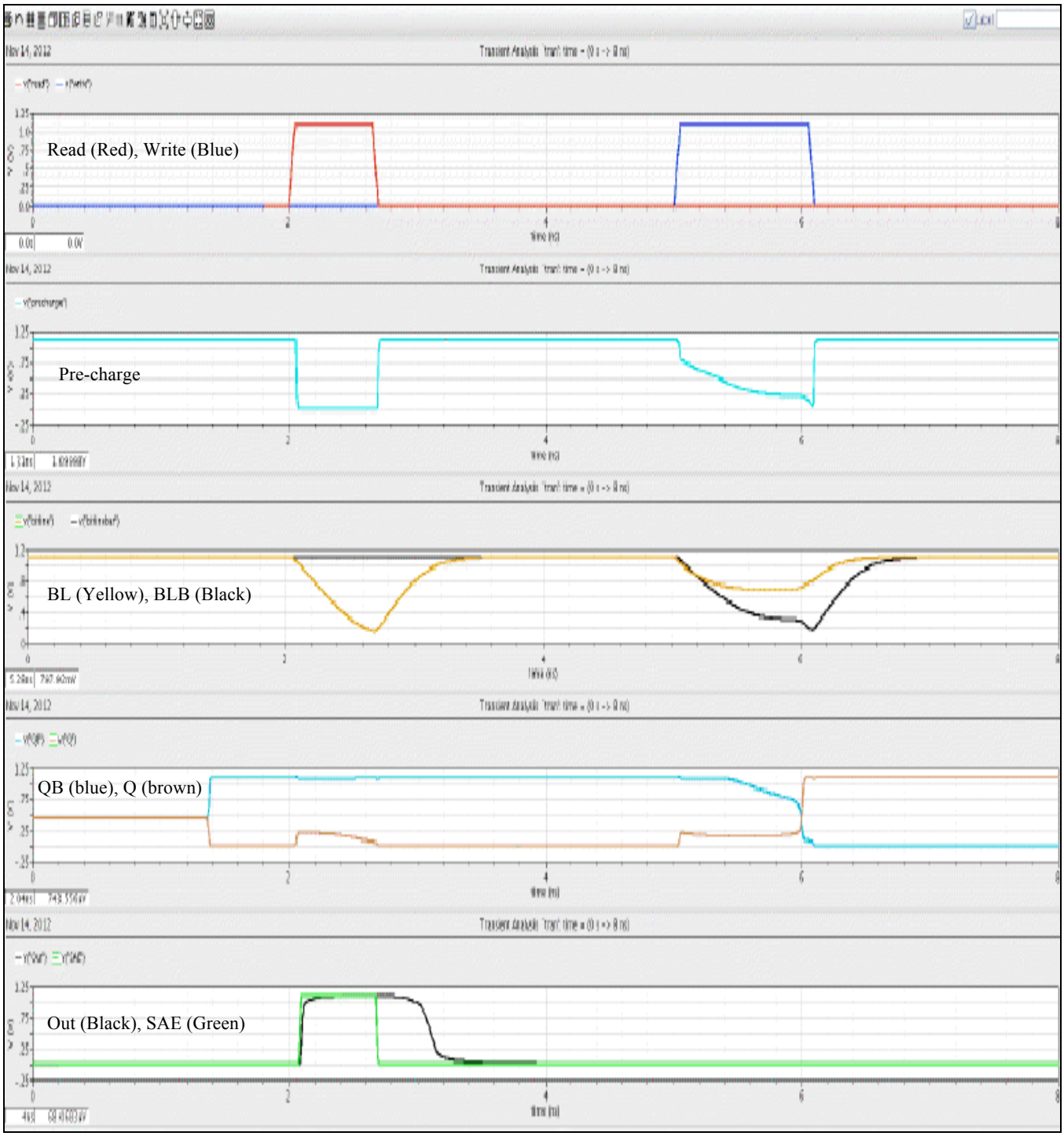


Figure 4. Array of 4 Bit Cells, Layout

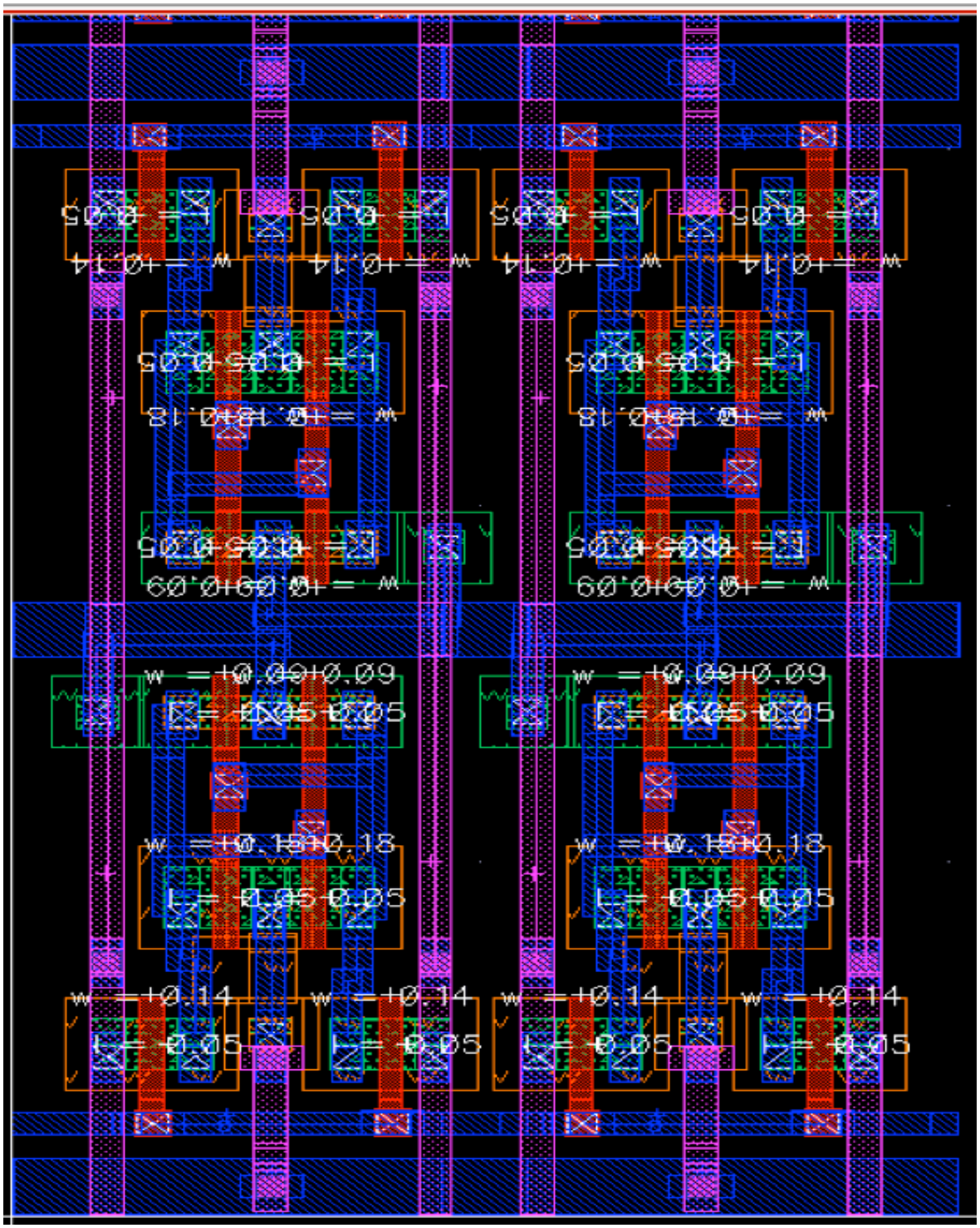


Figure 5. Single Bit Cells, Layout

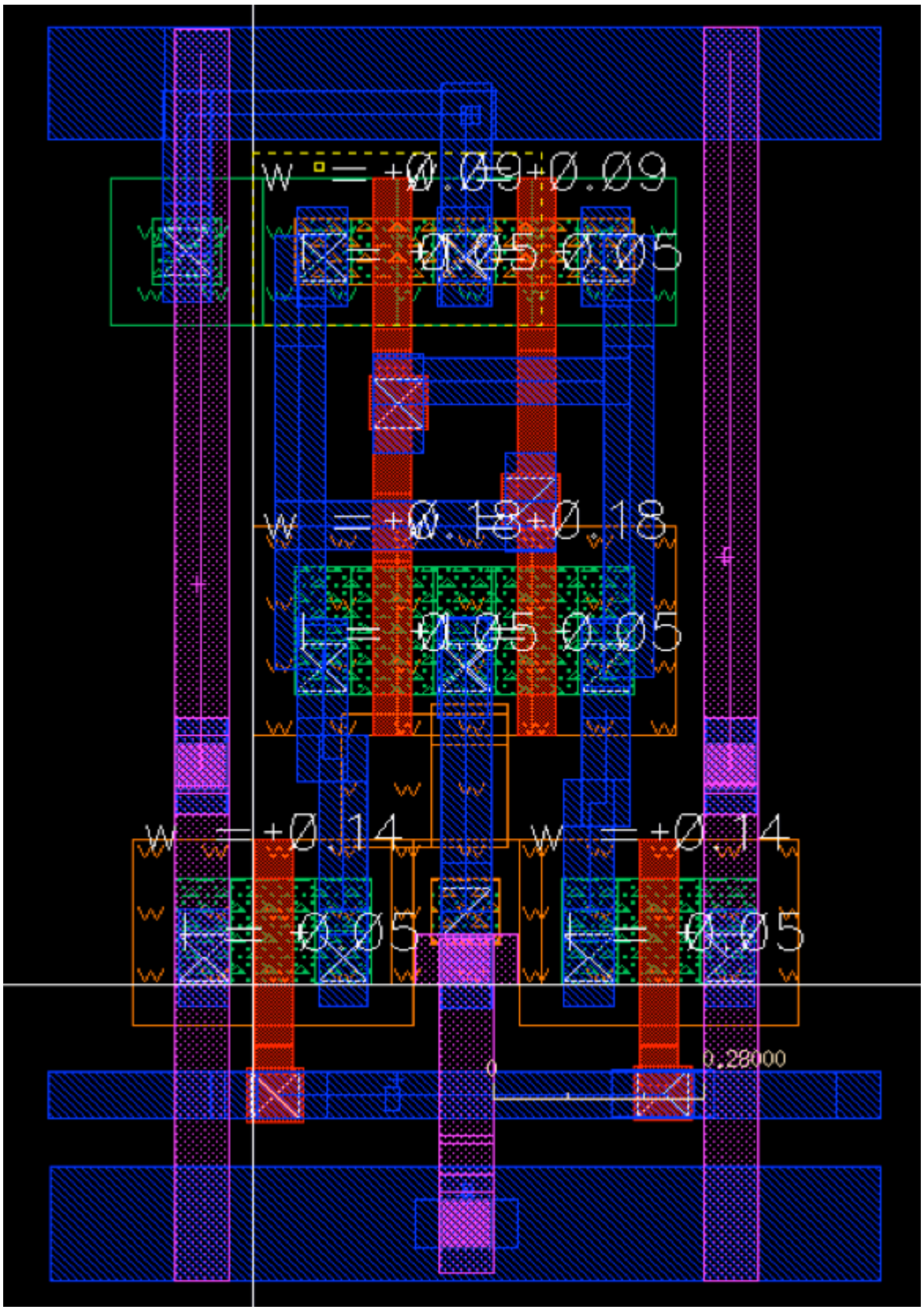


Figure 6. SNM Butterfly Curves, Hold Operation

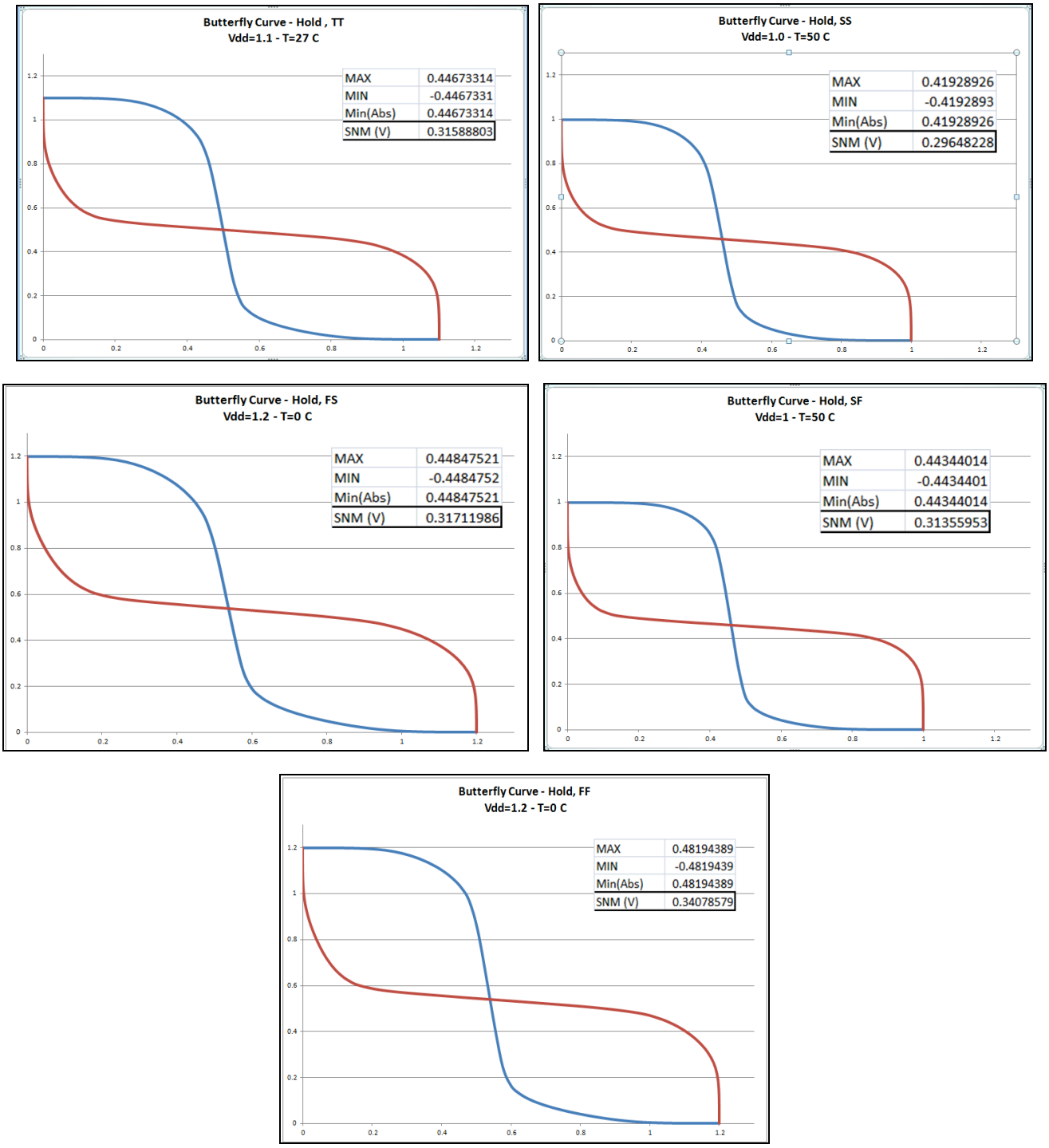
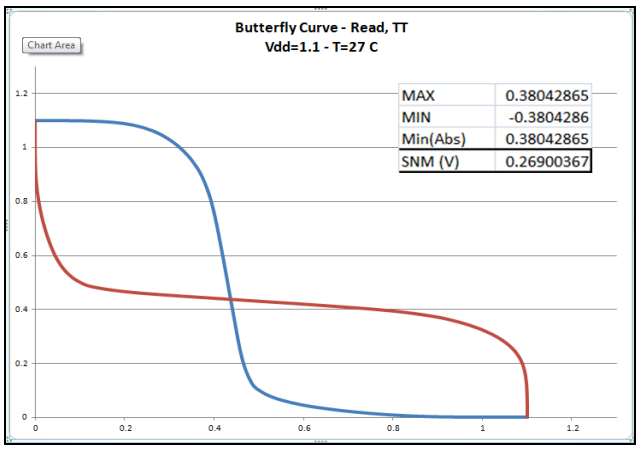
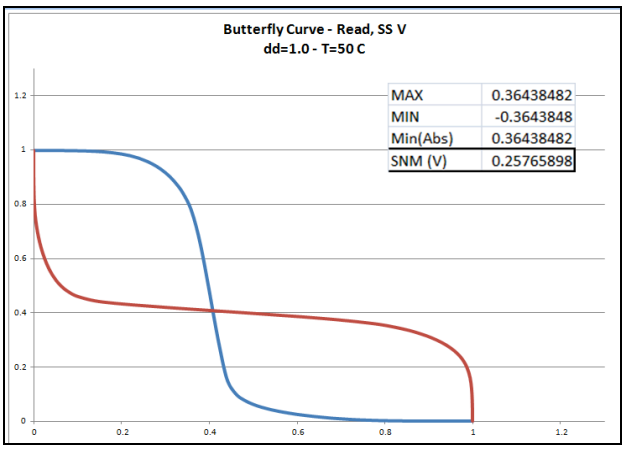
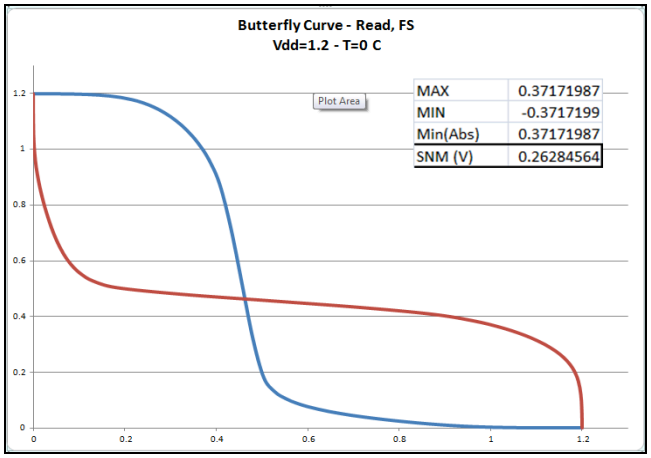
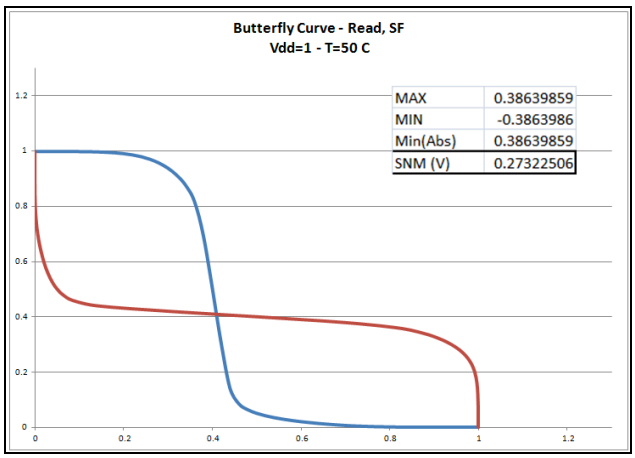


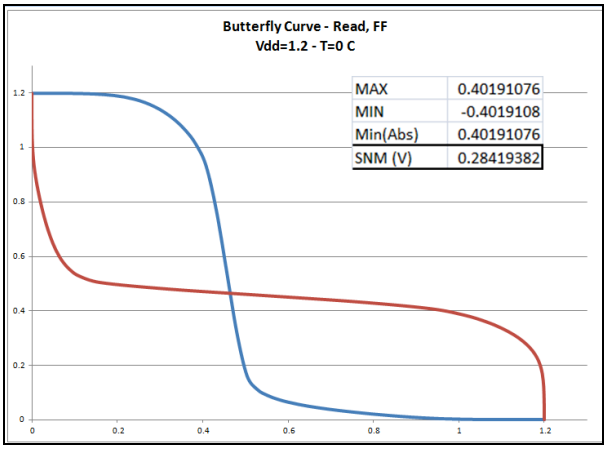
Figure 7. SNM Butterfly Curves, Read Operation


Butterfly Curve - Read, TT
Vdd=1.1 - T=27 C
Chart Area
MAX 0.38042865
MIN -0.3804286
Min(Abs) 0.38042865
SNM (V) 0.26900367


Butterfly Curve - Read, SS V
dd=1.0 - T=50 C
MAX 0.36438482
MIN -0.3643848
Min(Abs) 0.36438482
SNM (V) 0.25765898


Butterfly Curve - Read, FS
Vdd=1.2 - T=0 C
Plot Area
MAX 0.37171987
MIN -0.3717199
Min(Abs) 0.37171987
SNM (V) 0.26284564


Butterfly Curve - Read, SF
Vdd=1 - T=50 C
MAX 0.38639859
MIN -0.3863986
Min(Abs) 0.38639859
SNM (V) 0.27322506


Butterfly Curve - Read, FF
Vdd=1.2 - T=0 C
MAX 0.40191076
MIN -0.4019108
Min(Abs) 0.40191076
SNM (V) 0.28419382